# DMX512 Decoding and Drive IC UCS512C1 Series

**Functional Description:**

UCS512C1 series is DMX512 parallel protocol LED driver chip at the grayscale level 65536 with optional channel 1/2/3/4high precision constant current output. UCS512C1 series decoding technology accurately decodes DMX512 signals, is compatible with and expands 512 protocol signals. UCS512C1 series fully adaptively decodes DMX512 signals with the transmission frequency within 200K-750K, without any speed setting, and can address up to 4096 channels. UCS512C1 series has a built-in E2PROM, and various parameters can be set in E2 without external connection. The chip provides 4 high-precision constant current output channels, and the current of each channel can be independently adjusted in 16 levels through the software. With the 16K high port refresh rate, it greatly improves the screen refresh rate. The UCS512C1 series can expand the current driving capability by short-circuiting multiple sets of constant current output interfaces. It is mainly designed for LED lighting systems for building decoration and stage lighting effects, and is suitable for LED lighting systems that need to be connected in parallel. The abnormality of one chip does not affect the normal operation of other chips, so the maintenance is simple and convenient.

**Features:**

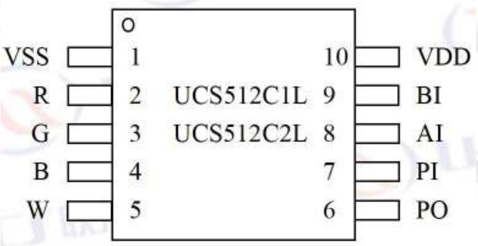
- Compatible with and expands DMX512(1990) signal protocol;
- Control mode: UCS512C1/C1L/C2/C2L are differential parallel connection, and UCS512CBL is single bus parallel connection
- Supports 4096 channels addressing
- Up to 12-bit precision self-adaptive decoding technology, accurately self-adaptively decodes DMX512 signals with a signal transmission rate of 200K ~ 750kbps
- The built-in 485 module has the advantages of high differential signal resolution and high differential input impedance, which can greatly enhance the load capacity
- Write parameter mode: Cascade write parameter, parallel write parameter
- Parameters set for UCS512C1 series: 1. Power-on lighting status + field selection + no signal lighting status 2. Current tap position
- Power-on lighting status selection parameters: You can choose any grayscale combination of the 4 output ports of RGBW after power-on
- Field selection parameters: 1, 2, 3, and 4 fields can be selected, and selecting the appropriate field can reduce the amount of data transmission while expanding the current
- No signal lighting parameters: Set whether the screen will keep the last frame or return to the color of the power-on lighting when there is no signal in1.5S
- Current: 2.4mA-20.4mA;16 tap positions settable
- UCS512C1/C1L and 512CBL are gray scale level 65536, gamma correction 2.2
- UCS512C2/C2L is gray scale level 256
- R/G/B/W four-bit constant current output channel, ±5% high-precision current difference between chips
- Port refresh rate up to 16K, no streaks for mobile phone/camera shooting
- A built-in 5V voltage regulator, RGBW output port withstand voltage 30V
- A built-in patented S-AI anti-jamming module, greatly enhancing the anti-jamming capability
- Output channel hysteresis to reduce inrush current interference
- Industrial grade design, stable performance

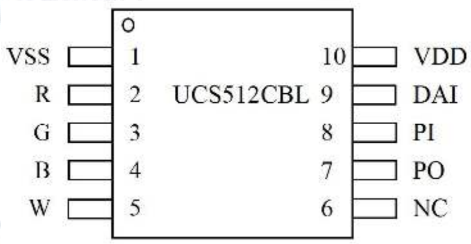
**Application Scope:**

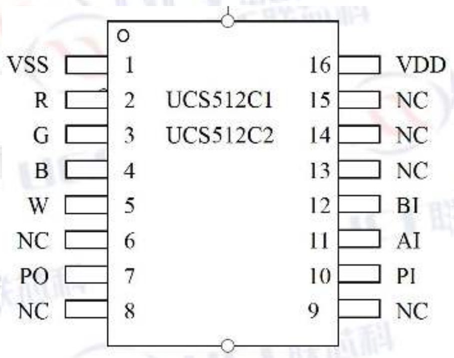
Point light sources, strip lights, wall washer lights, stage lighting systems, indoor and outdoor video walls and decorative lighting systems

**Pin Diagrams:**

1. UCS512C1L/C2L(SOP10) 2.UCS512CBL(SOP10) 3.UCS512C1/C2(SOP16)




**Description of Pins**

| | UCS512C1L/UCS512C2L | |
|---|---|---|
| SN | Symbol | Functional description |
| 1 | VSS | Ground |
| 2~5 | RGBW | PWM output port |
| 6 | PO | Coding control line output |
| 7 | PI | Coding control line input, built-in pull-up |
| 8 | AI | Differential signal, positive |
| 9 | BI | Differential signal, negative |
| 10 | VDD | Power terminal, built-in 5V voltage regulator |

| | UCS512CBL | |
|---|---|---|
| SN | Symbol | Functional description |
| 1 | VSS | Ground |
| 2~5 | RGBW | PWM output port |
| 6 | NC | Null pin |
| 7 | PO | Coding control line output |
| 8 | PI | Coding control line input, built-in pull-up |
| 9 | DAI | DMX512 data input |
| 10 | VDD | Power terminal, built-in 5V voltage regulator |

| | UCS512C1/UCS512C2 | |
|---|---|---|
| SN | Symbol | Functional description |
| 1 | VSS | Ground |
| 2~5 | RGBW | PWM output port |
| 6 | NC | Null pin |
| 7 | PO | Coding control line output |
| 8 | NC | Null pin |
| 9 | NC | Null pin |
| 10 | PI | Coding control line input, built-in pull-up |
| 11 | AI | Differential signal, positive |
| 12 | BI | Differential signal, negative |
| 13 | NC | Null pin |
| 14 | NC | Null pin |
| 15 | NC | Null pin |
| 16 | VDD | Power terminal, built-in 5V voltage regulator |

**Maximum Rating** (Unless otherwise specified, Ta=25℃, Vdd=5V)

| Parameter | Symbol | Range | Unit |
|---|---|---|---|
| Logic supply voltage | $V_{dd}$ | -0.5～＋6 | V |
| Logic input voltage | $V_i$ | −0.5～Vdd＋0.5 | V |
| Output port withstand voltage | $V_{out}$ | 30 | V |
| RGBW output maximum current | $I_{out}$ | 20.4 | mA |

| | | | |
|---|---|---|---|
| VDD maximum clamp current | $I_{damp}$ | 25 | mA |
| Operating junction temperature | $T_j$ | −45～＋150 | ℃ |
| Storage temperature | $T_{stg}$ | −55～＋150 | ℃ |
| Thermal resistance from PN junction to environment (SOP16) | RθJA | 90 | ℃/W |
| Thermal resistance from PN junction to environment (SOP10) | RθJA | 125 | ℃/W |
| Maximum power consumption (SOP16) | $P_d$ | 900 | mW |
| Maximum power consumption (SOP10) | $P_d$ | 600 | mW |
| anti-static electricity (HBM) | ESD | 6000 | V |

Note 1: The maximum limit value means that the chip may be damaged beyond the operating range. When operating within the extreme parameters, the device will function properly, but individual performance indicators cannot be fully guaranteed.

Note 2: RθJA is measured on a single-layer thermally conductive test board according to JEDEC JESD51 thermal measurement standard under the TA=25℃ natural convection.

Note 3: The maximum power consumption is limited by the chip junction temperature, and the maximum output power will decrease when the ambient temperature increases, which is also determined by the junction temperature $T_{JMAX}$, ambient temperature $T_A$ and RθJA. The maximum allowable power dissipation is $P_D = (T_{JMAX}-T_A)/$ RθJA or the lower value of the values given in the limits

**Recommended Operating Range** (unless otherwise specified, Ta=−40～+85℃, Vdd=5V)

| Parameter | Symbol | Minimum | Typical | Maximum | Unit | Test condition |
|---|---|---|---|---|---|---|
| Logic supply voltage | Vdd | 3 | 5 | 5.7 | V | - |

**Electrical Parameters** (unless otherwise specified, Ta=−40～+85℃, Vss=0V, Vdd=4.5～5.5V)

| Parameter | Symbol | Minimum | Typical | Maximum | Unit | Test condition |
|---|---|---|---|---|---|---|
| Clamp voltage | $V_{dd}$ | 4.8 | | 5.5 | V | $V_{in}$=12V, dropping resistor 1K |
| Dynamic current consumption | $I_{DDdyn}$ | | 3 | | mA | Po off |
| High level output current | $I_{poh}$ | | 17 | | mA | $V_{po}$ = 4.6V |
| Low level output current | $I_{pol}$ | | 25 | | mA | $V_{po}$ = 0.4V |
| High level input voltage | $V_{ih}$ | 0.7 $V_{dd}$ | | | V | DPI/DAI high level |
| Low level input voltage | $V_{il}$ | | | 0.3 $V_{dd}$ | V | DPI/DAI low level |
| Differential input common mode voltage | Vcm | -7 | | 12 | V | $V_{dd}$=5V |

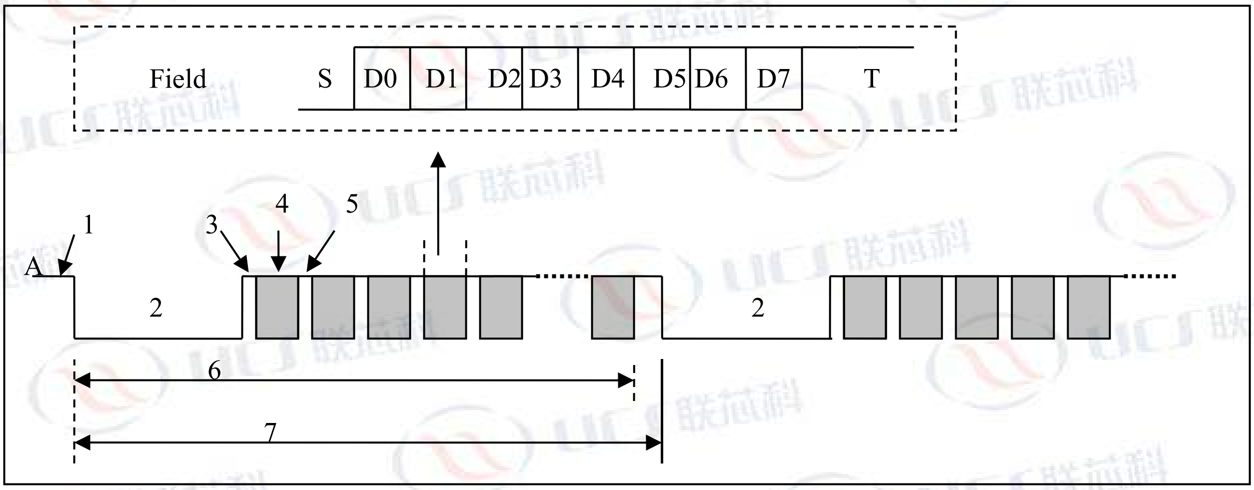
| | | | | | | |
|---|---|---|---|---|---|---|
| Differential input current | $I_{AB}$ | | | 28 | uA | $V_{dd}$=5V |
| Differential input threshold voltage | $V_{th}$ | -0.2 | | 0.2 | V | $V_{dd}$=5V |
| Differential input hysteresis voltage | $\triangle V_{TH}$ | | 70 | | mV | $V_{dd}$=5V |
| A/B port pull-down resistance | $R_{downAB}$ | | 190 | | KΩ | $V_{dd}$=5V |
| A port pull-up resistance | $R_{upA}$ | | 800 | | KΩ | $V_{dd}$=5V |
| Output port knee point voltage | $V_{ds-s}$ | | 0.8 | | V | R/G/B/W=20.4mA |
| Current offset (between chips) | $D_{Iout}$ | | | ±5.0 | % | $V_{ds}$=1V，$I_{out}$=20.4mA |
| OUT output current change | $\%dV_{ds}$ | | ±0.5 | | %/V | 1V<$V_{ds}$<3V |
| | $\%dV_{dd}$ | | ±1.0 | | %/V | 4.5V<$V_{dd}$<5.5V |
| | $\%dT_A$ | | ±3.0 | | %/℃ | $T_A$=-40~+85℃ |

**Switching Characteristics** (Unless otherwise specified, Ta=−40～+85℃, Vss=0V, Vdd=4.5～5.5V)

| Parameter | Symbol | Minimum | Typical | Maximum | Unit | Test condition |
|---|---|---|---|---|---|---|
| Port refresh rate | $F_{pwm}$ | | 16 | | KHz | $I_{OUT}$=20mA |
| Data transfer rate | F | 200 | | 750 | Kbps | |
| Input capacitance | Ci | - | - | 15 | pF | |

**Communication Data Protocol:**

UCS512C1 series data reception is compatible with the standard DMX512 (1990) protocol and extended DMX512 protocol. It self-adapts to the decoding with the data transmission rate of 200kbps to 750K. The protocol waveform is as follows: The chip is inputted by AB differentially, the timing waveform of A is drawn in the figure, and B is opposite to A.




| No. | Description | Minimum | Typical value | Maximum | Unit |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| | Bit rate | 200 | 250 | 500 | Kbps |
| | Bit time | 5 | 4 | 2 | us |
| S | Start bit | 5 | 4 | 2 | us |
| D0~D7 | Data bit | 5 | 4 | 2 | us |
| T | 2-digit stop bit | 10 | 8 | 4 | us |
| 1 | Mark before reset | 0 | | 1000000 | us |
| 2 | Reset signal | 88 | | 1000000 | us |
| 3 | Mark after mark | 8 | | 1000000 | us |
| 4 | Field (note 1) | 55 | 44 | 22 | us |
| 5 | Idle time between fields | 0 | | 1000000 | us |
| 6 | Length of data packet | 1024 | | 1000000 | us |
| 7 | Reset signal interval | 4096 | | 1000000 | us |

Note1: The field has 11 bits in total, including 0 start bits, 8 data bits and 2 stop bits. The 0 start bit is at the low level, and the stop bit is at the high level. When the data in the data bit is 0, the corresponding time period is at the low level; if it is 1, the corresponding time period is at the high level. 0 start bit, stop bit and data bit must have the same bit duration.

**Instructions for IC Receiving:**

1. When the reset signal appears on the AB line, the IC will enter the receiving ready state. Clear the address counter.
2. The first field in the data packet is the start field, and its 8-bit data must be "0000_0000". This field is not used as the display data. The valid field for display starts from the second field, and the second field of the 512 data packet is the first field of valid data. The data transmission frequency that the IC can self-adapt to is 200K-750K. The field durations corresponding to different frequencies are different. However, for the transmission frequency of 200K or 750K, it is only necessary to ensure that the duration of all valid fields is the same as that of the initial field. It shall be noted that, the higher the sending rate, the shorter the bus length must be, so it is recommended that the sending frequency should not exceed 500K.
3. The IC determines and intercepts the corresponding field in the 512 data packet according to its E2 address. If the chip address is 0000_0000_0000, it will intercept from the first valid field of the data packet; if the chip address is 0000_0000_0001, it will intercept from the second valid field of the data packet. The number of fields used by the chip is set by the control system.

**Functional Description:**

**Coding Method**

**Cascaded coding:** For the conventional coding method, different addresses can be written into each IC, but ensure that the coding line is normal.

**Parallel coding:** All ICs on a bus are written to the same address, and the coding line fault does not affect the address writing.

## Parameter Writing Method

**Cascaded parameter writing:** You can write different parameter values into each IC, but ensure that the coding line is normal

**Parallel parameter writing:** Only the same parameter values can be written into all ICs on one bus, and the failure of the coding line does not affect the parameter writing.

## Parameters Description

**Power-on lighting:** RGBW grayscale of each channel can be self-defined

**1.5S no signal status:** You can choose to restore the power-on lighting status or keep the last frame

**Current range:** **The current of each channel of RGBW can be independently set from 2.4mA to 20.4mA, with 16 levels**

| SN | Output current (mA) |
|---|---|
| 0 | 2.4 |
| 1 | 3.6 |
| 2 | 4.8 |
| 3 | 6 |
| 4 | 7.2 |
| 5 | 8.4 |
| 6 | 9.6 |
| 7 | 10.8 |
| 8 | 12 |
| 9 | 13.2 |
| 10 | 14.4 |
| 11 | 15.6 |
| 12 | 16.8 |
| 13 | 18 (default value) |
| 14 | 19.2 |
| 15 | 20.4 |

**Fields Selection:**

| Mode | Effect |
|---|---|
| 4-field mode | 4 fields are intercepted to correspond to R, G, B and W, respectively |
| 3-field mode | 3 fields are intercepted to correspond to R, G and B. W is closed |
| 2-field mode | 2 fields are intercepted to correspond to RG and BW |
| 1-field mode | 1 field is intercepted to correspond to RGBW |

In the above table, the 1-field mode and 2-field mode can realize the function of expanding the current with the minimum amount of data transmission. For example, in the 1-field mode (generally the single color application), 4 output pins of RGBW can be connected in parallel for using. At this time, the maximum output current can reach 4 times the single-channel current. The above fields are only required when the current expansion is required. When the current expansion is not required, the 4-field mode can be directly selected.

**Lighting after Coding and Parameters Writing**

| EEPROM writing operation | | | Lighting description |
|---|---|---|---|
| Successful write-in | Address writing | Overall writing | RGBW |
| | | Cascaded writing | First light: RG; non-first light: RGBW |
| | Writing power-on self-defining grayscale, 1.5S no signal status, number of fields | Overall writing | Write-in grayscale |
| | | Cascaded writing | Write-in grayscale |
| | Current writing | Overall writing | RGBW |
| | | Cascaded writing | First light: RG; non-first light: RGBW |
| Unsuccessful write-in | | | Black |

**S-AI anti-interference patented technology:** One of our patented technologies used in high-speed communication interface IC; through an embedded algorithm module, a certain range of differential mode interference signals was filtered. It forms complementarity with the common mode anti-interference capability of the differential bus to some extent and applies to the engineering environment with large interference

**Factory Default Values**

| Model | UCS512C1/C1L | UCS512C2/C2L | UCS512CBL |
|---|---|---|---|
| Power-on self-defined grayscale | B（22%） | B（22%） | B（22%） |
| 1.5S no signal status | The last frame is kept | The last frame is kept | The last frame is kept |
| Number of fields | 4 | 4 | 4 |
| Current | 18mA | 18mA | 18mA |

**Notes for Differential Bus Connection:**

1. There must be a common ground between the controller and the IC and between the ICs to prevent the IC from being broken down by excessive common-mode voltage. When a shielded wire is used, the shielding layer can be used as a common ground wire to reliably connect multiple IC nodes, and reliably connect to the ground at one point. Both ends or multiple ends cannot be connected to the ground at the same time.
2. The protection resistors connected in series between the A and B lines on the board and the IC must be the same, and the AB lines on the board shall be wired side by side. There shall be no other wiring or components between the AB lines.

3.The twisted pair wires are generally used for the AB bus and ordinary sheathed wires can also be used, but copper wires shall be purchased. Shielded twisted pair wires can be used in the shared project of strong and weak current wiring ducts, near the launch tower or in areas where lightning is frequent to reduce interference and lightning impact.

4. In the 485 bus, the distance between the 485 nodes and the trunk should be minimized. Generally, it is recommended that the 485 bus should be in the hand-in-hand bus topology. Structures with main lines and branch lines, such as star structure or tree structure, will generate reflected signals and affect the quality of 485 communication. If the wiring structure of the main line and branch line has been adopted during the construction and the length of the branch line exceeds 1 meter, it is recommended to use a 485 repeater to make a 485 bus fork at the position where each branch line exceeds 1 meter. The repeater shall be close to the main line. Multiple branches can also be connected separately using a multi-outlet 485 repeater.

5. With the extension of the transmission distance, the 485 bus will generate echo reflection signal. If the transmission distance of the 485 bus is long, it is recommended to connect a 120 ohm terminal matching resistor on the AB line at the end of the 485 communication during construction

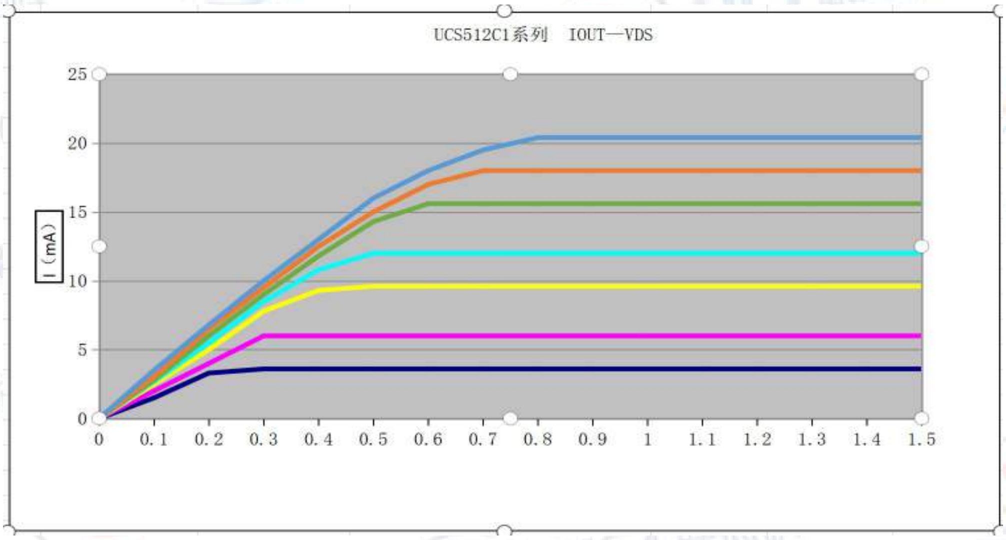
**Constant Current Curve:**

UCS512C1 series has excellent constant current characteristics, and the current difference between channels and even between chips is very small.

(1): The maximum current error between channels is ±3%, and the maximum current error between chips is ±5%.

(2): When the load terminal voltage changes, the output current will not be affected, as shown in the figure below

(3): The following figure shows the curve relationship between the current I of the output port and the voltage Vds applied to the port. It can be concluded that, the smaller the I current is, the smaller the Vds is required in the constant current status.




系列

Series

**Voltage Divider Resistor Selection:**

**Power consumption calculation:** $P=P_{RGB}+P_{VDD}$

Take 4 channels of 20.4mA per channel as an example. When the output pin voltage drop (Vds) is 3V, then the power consumption at the highest grayscale on the IC:

$P=P_{RGB}+P_{VDD}$=4*3V*20.4mA+5V*10mA=0.25+0.05=0.3W

Note: The actual power consumption shall not exceed the maximum allowable power consumption, and the maximum allowable power consumption PD is determined by the power consumption rating and ambient temperature and heat dissipation conditions

**Calculation of Voltage Divider Resistance:**

VCC—N*Vled-min—VR < Vds-max

VR=I*R R refers to the voltage divider resistance

R >（VCC—-N*Vled-min—Vds-max)/I

VCC refers to the power supply voltage, $V_{led\text{-}min}$ refers to the minimum turn-on voltage of the lamp beads, N refers to the number of lamp beads in series, $V_{ds\text{-}max}$ refers to the maximum voltage of each output pin, and I refers to the set constant current value.

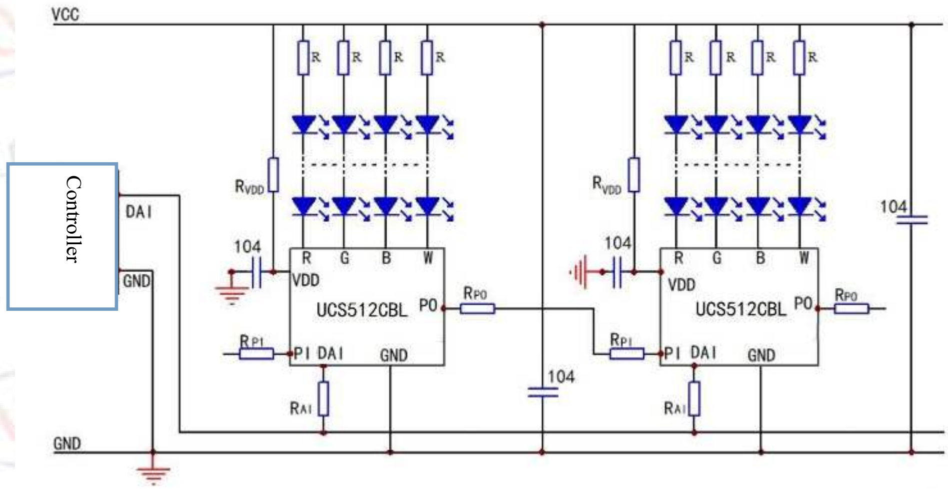
Note: Resistor power dissipation shall be considered when a voltage divider resistor is selected.

**Application Diagram 1: UCS512C1, 512C1L, UC S512C2 and UCS512C2L**

**Values Selection of Components:**

| Component | 24V | 12V | 5V |
|---|---|---|---|
| $R_{VDD}$ | 2K | 750 | 80 |
| $R_{PI}$ | 500-1K | 500-1K | 500-1K |
| $R_{PO}$ | 500-1K | 500-1K | 500-1K |
| $R_A$ | 5K-10K | 5K-10K | 5K-10K |
| $R_B$ | 5K-10K | 5K-10K | 5K-10K |

**Application Diagram 2: UCS512CBL**




**Values Selection of Components**

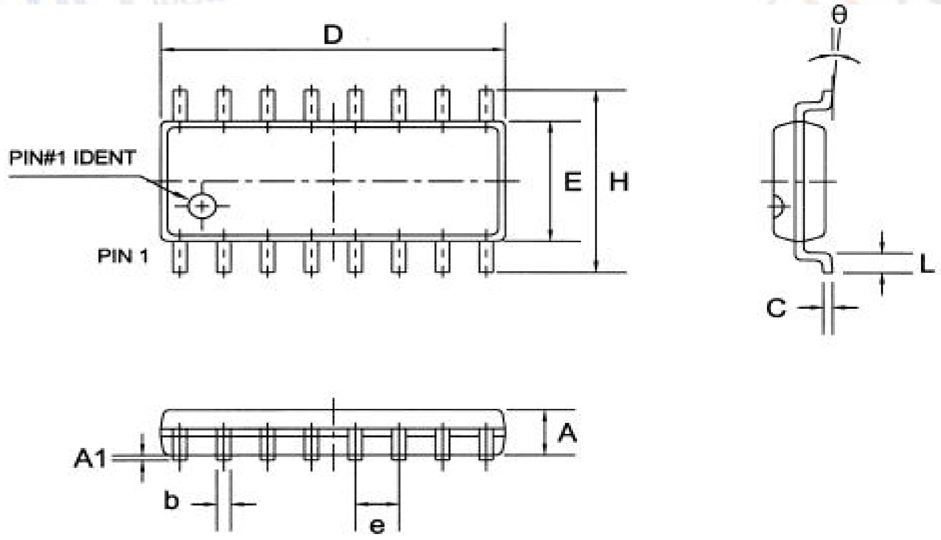
| Component | 24V | 12V | 5V |
|---|---|---|---|
| RVDD | 2K | 750 | 82 |
| RPI | 500-1K | 500-1K | 500-1K |
| RPO | 500-1K | 500-1K | 500-1K |
| RA | 10K | 10K | 10K |

**Application of DMX512 and Expansion Protocol on Lamps**

| Component | Transmission frequency | Number of channles on the bus | Frame frequency |
|---|---|---|---|
| Standard protocol | 250K | 512 | 44 |
| Channel expansion | 250K | 1024 | 22 |
| Channel expansion | 250K | 1536 | 15 |
| Transmission frequency and channel expansion | 500K | 1024 | 44 |
| Transmission frequency and channel expansion | 500K | 1536 | 30 |
| Transmission frequency and channel expansion | 500K | 2048 | 22 |

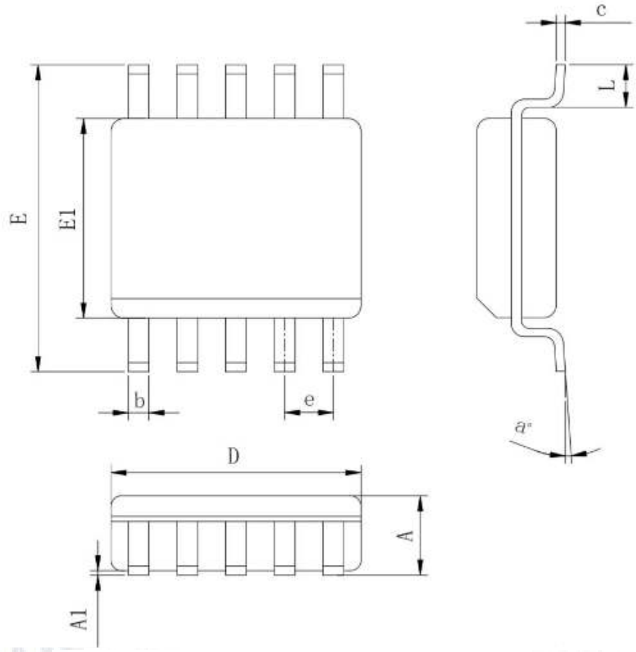
**Encapsulation Outline Drawing and Dimensions**

SOP16




| Symbol | Dimensions In Millimeters | | | Dimensions In Inches | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 1.30 | 1.50 | 1.70 | 0.051 | 0.059 | 0.067 |
| A1 | 0.06 | 0.16 | 0.26 | 0.002 | 0.006 | 0.010 |
| b | 0.30 | 0.40 | 0.55 | 0.012 | 0.016 | 0.022 |
| C | 0.15 | 0.25 | 0.35 | 0.006 | 0.010 | 0.014 |
| D | 9.70 | 10.00 | 10.30 | 0.382 | 0.394 | 0.406 |
| E | 3.75 | 3.95 | 4.15 | 0.148 | 0.156 | 0.163 |
| e | — | 1.27 | — | — | 0.050 | — |
| H | 5.70 | 6.00 | 6.30 | 0.224 | 0.236 | 0.248 |
| L | 0.45 | 0.65 | 0.85 | 0.018 | 0.026 | 0.033 |
| θ | 0° | — | 8° | 0° | — | 8° |

SOP10




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | -- | -- | 1.75 |
| A1 | 0.10 | -- | 0.23 |
| b | 0.30 | -- | 0.40 |
| c | 0.19 | -- | 0.25 |
| D | 4.70 | 4.90 | 5.10 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.70 | 3.90 | 4.10 |
| e | 1.00 BSC | | |
| L | 0.40 | -- | 0.80 |
| a° | 0° | -- | 8° |

**Version No.**

| Version | Date of issue | Revision description |
|---|---|---|
| VER1.0 | 2022-5-25 | Issue of the first version |
| VER1.5 | 2022-8-27 | Contents correction |